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Issue	Date	Change Description
Version 1.0	Feb 26 th 2020	Initial Issue

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List of Abbreviations (if applicable)

- WFE: Wavefront error (effect of the SFE on a reflected beam)
- SFE surface front error (shaping of the optical surface)

1 Introduction

In 2017, Winlight Optics (WO) delivered an image slicer demonstrator for SOLARNET. The configuration was limited to the slices thickness we were capable to polish in 2015 (date of the beginning of the project), it means around 100 μm thick.

Now, the resolution of the next generation image slicer has to be increased to meet 50 μm / 70 μm of slices thickness. This report shows the results of the slices thinning we will be capable to do for the future slicer for EST.

Note that during the project WINLIGHT OPTICS and WINLIGHT SYSTEM have been merged and the remaining institution is now WINLIGHT SYSTEM.

WINLIGHT-SYSTEM document code: WS3128-003-RAP001-B

2 Applicable documents

[AD1] Grant Agreement-824135-SOLARNET

[AD2] Research and innovation actions Annex 1 part A WP6

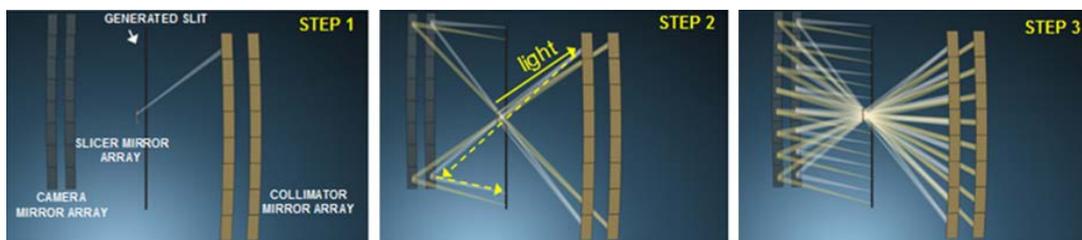
3 Reference documents

[RD1] Test plan for slices thinning: WO4688-001-TPL002-A

4 Overview of the existing image slicer

4.1 General description

MuSiCa for GRIS is a 1:1 telecentric system. It is composed by three arrays of mirrors: slicer mirror array, collimator mirror array and camera mirror array. The slicer mirrors are flat, they are located at the telescope image focal plane and each slicer mirror has a different orientation (tilt X, tilt Y) to reflect a part of the entrance field of view and send it to a collimator mirror. The optical path of each sliced part of the field of view is described by the reflection of the beam in one mirror of each array to generate a part of the output slit, what is known as ‘mini-slit’. The second optical element is the collimator mirror array, composed by eight spherical mirrors. In front of the collimator mirrors the camera mirrors are placed, which are also spherical. Collimator and camera mirrors have antisymmetric correspondences, so that the intermediate pupil images, generated between them, lie at the same position and are all overlapped. At the pupil position a mask is placed to avoid the contribution of scattered light. Figure 1 represents the different steps in the optical path of MuSiCa, from the slicer mirror array (at the telescope image focal plane) until the output slit and it shows the optical components (step 1). In the second step the beam reflected by a slicer mirror is sent to a collimator mirror, which collimates it; a pupil image is generated at its focal length, between the collimator and the camera mirror arrays; the camera mirror focuses it and generates its image at its focal length. This image, a mini-slit, is a piece of the output slit. The final slit is generated alternating focusing beams of each one of the two columns of camera mirrors to compensate the angles of incidence and improve the optical quality. The images of each part of the sliced field of view are aligned composing the output long slit (step 3). The pupil images are overlapped in an intermediate plane between the slicer mirror array and the generated slit. Once the IFU is coupled to the GRIS spectrograph at GREGOR solar telescope, the pupils associated to the eight different slices of the entrance field of view should be overlapped at the diffraction grating position.

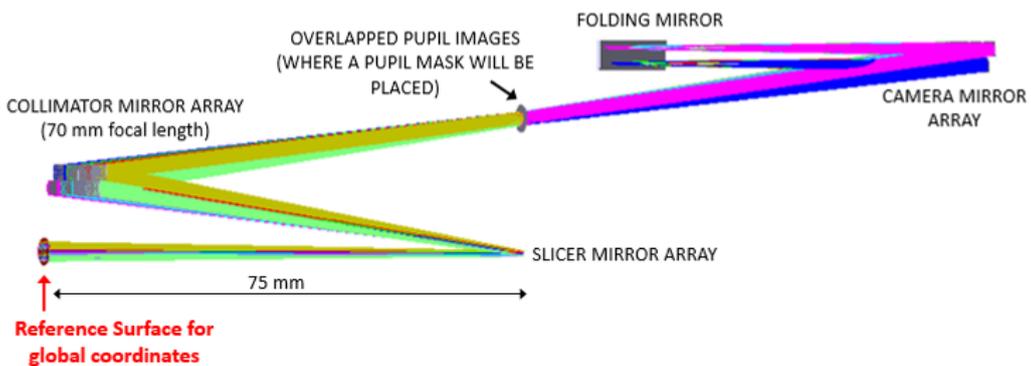


4.2 Requirements

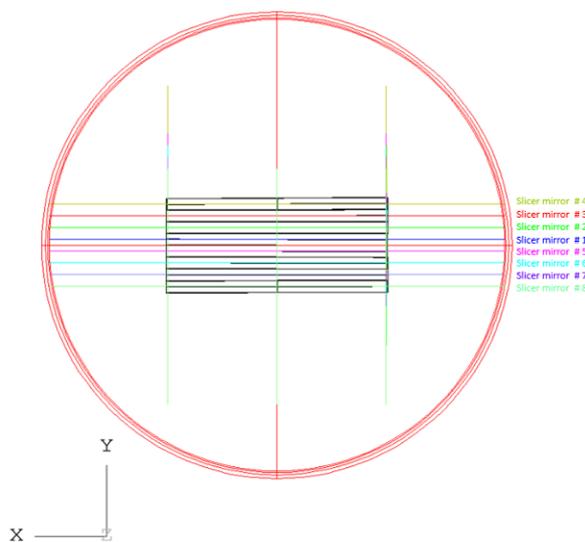
The prototype image slicer is coupled to GRIS [1], the GREGOR infrared spectrograph. GRIS is a long slit spectrograph that operates in the near-infrared, from 1 to 2.3 μm with very high resolution ($R \sim 500,000$) for measurements of the photospheric and chromospheric magnetic field. It presents a Czerny-Turner layout using off-axis parabolic mirrors with a focal length of 6 meters and an echelle diffraction grating with 316 grooves/mm and a blaze angle of 63.4°.

SPECIFICATIONS AND REQUIREMENTS FOR THE IFU PROTOTYPE	
Input focal-ratio	F/37.67 (valid for F/37.67 to F/39.79)
Output focal-ratio	F/37.67
Magnification	1
Number of slices	8
Slices width	100 μm
Number of output slits	1
Optimum illumination	telecentric

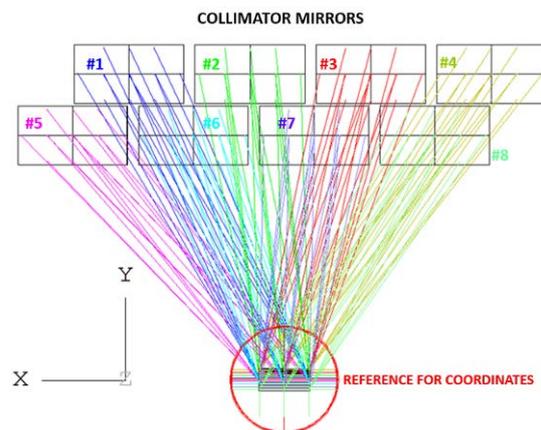
Specifications and requirements for the IFU prototype design.



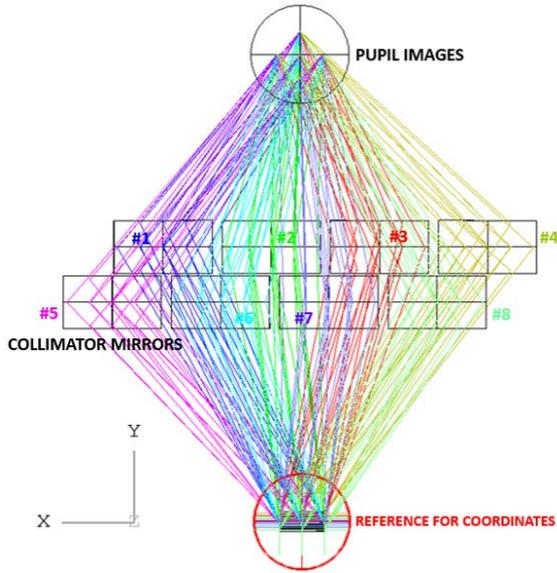
Reference surface for global coordinates at the border of the zerodur platform



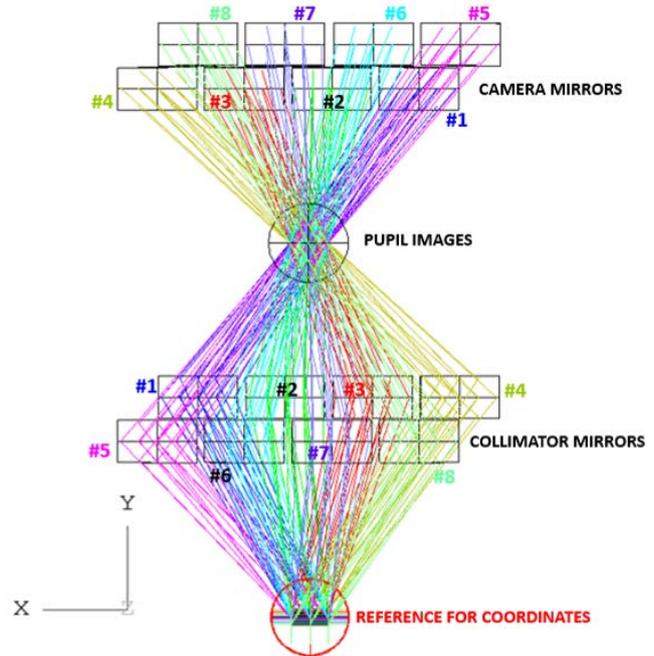
The eight slicer mirrors with respect to the surface global coordinate reference



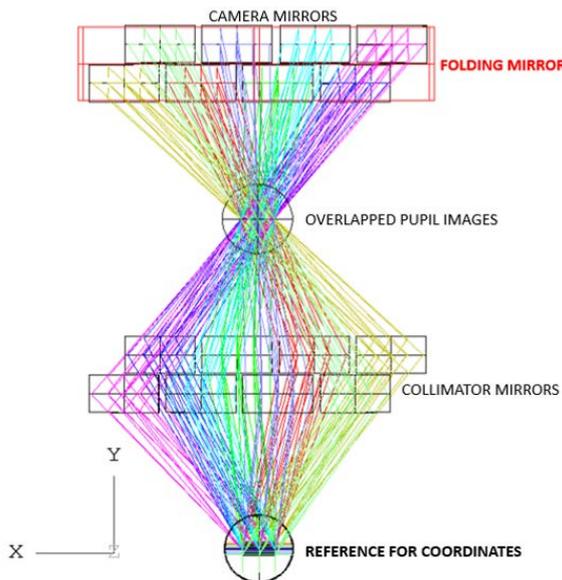
Slicer mirror array and collimator mirrors with respect to the reference surface (red) and its defined axes.



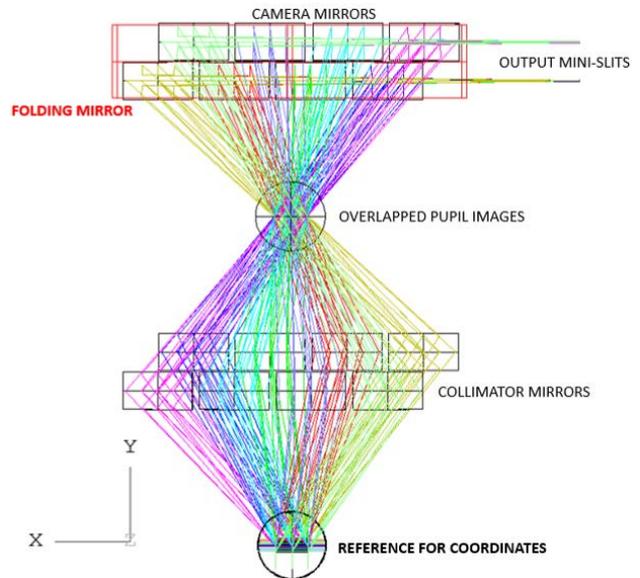
Slicer mirrors, collimator mirrors and the overlapped pupil images with respect to the surface defined as the reference for global coordinates.



Slicer mirrors, collimator mirrors, the overlapped pupil images and the camera mirrors with respect to the surface defined as the reference for global coordinates (in red).

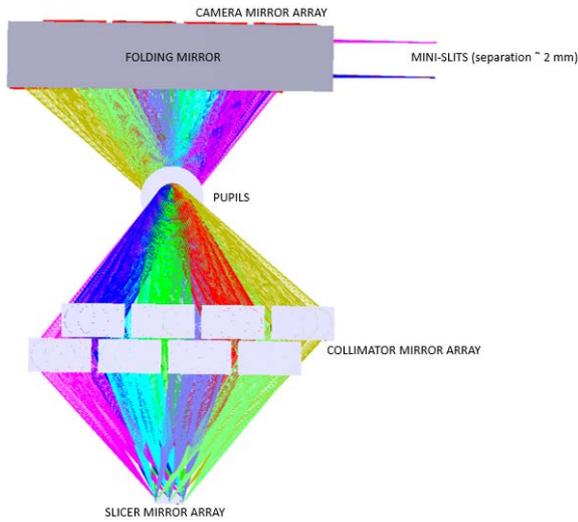


The difference of this layout with respect to the previous one is that the folding mirror is shown here

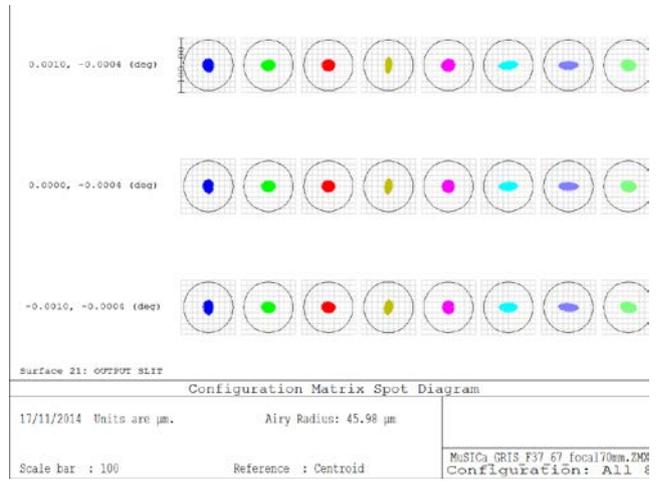


Layout of the image slicer including all its components and the reference for global coordinates

4.3 Layout and optical quality



Front view of the image slicer prototype.



Spot diagram of the IFU with an optical quality limited by diffraction.

4.4 Delivered image slicer demonstrator with 100 μm slices

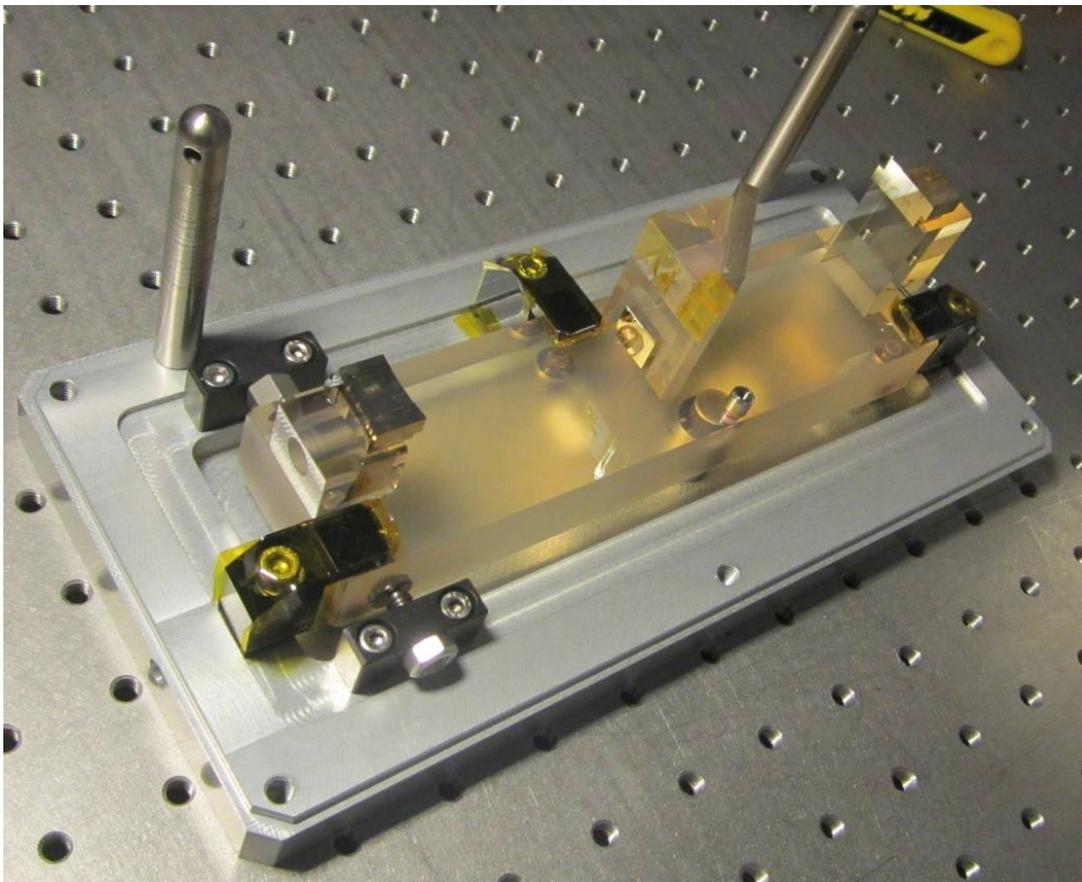
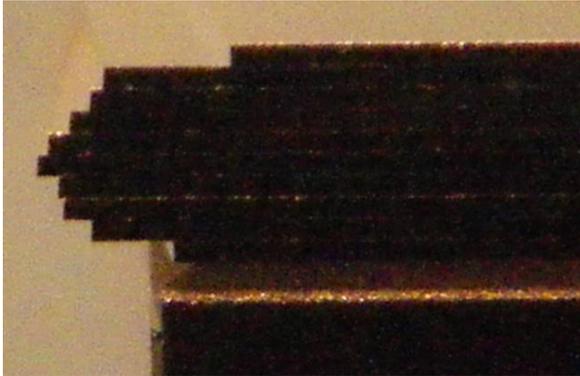
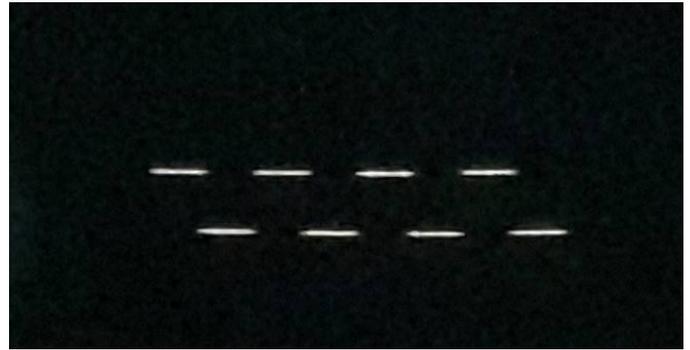


Image slicer installed at GRIS by WINLIGHT



Slices 100µm thick done by WINLIGHT



Final mini slit array

5 Work package description

Work package number	WP6
Lead beneficiary	IAC
Work package title	Advanced instrumentation development
Start month 1	End month 48
Participants	IAC, KIS, SU, INAF, UNITOV, MPG, USI/IRSOL, WO, NAOJ, ADS, BDP E&M

Development of instrumentation to improve the existing solar telescopes and with possible application to the future large aperture solar telescopes. The instrumentation developments included in this WP are the following. The WP6 is divided into 4 subWPs according to its objectives but we are only concerned by the first subWPs:

- Improvements of techniques of image slicers for 2D spectroscopy
- Microlens-fed spectrograph
- Design concept of a Narrow-Band Tunable-Filter Imager for EST
- Absolute high precision polarization measurements

6 Results of the tests

The thinning process was not easy to do; we had to consider during the process several concerns listed below:

1. Thinning the elements keeping the future optical contacting surface as flat as possible
2. Keeping a good reliability during the final thinning
3. Manipulate the slices and be capable to stack it

6.1 Stressless thinning process

Various process parameters have been experimented to find a solution to thin the slices without stress. To determine the influence of each parameter and exclude potential random parameters, several runs have been done. A total of 50 slices section 20 x 30 x 1.5mm have been processed (25 Zerodur– 25 Fused silica).

Stress-less thinning process results:

There is no processing difference between Zerodur and Fused silica. Using the same polishing process, both materials have very similar behaviour when polishing.

6.1 Reliability for the final thinning and the shaping

When the best process has been chosen, we began to demonstrate the manufacturing process using slices cut to the actual final dimension. This leads to a better thickness/surface ratio (10x15mm).

As we did not observe any processing difference between Fused silica and Zerodur, we chose to continue with Zerodur material only.

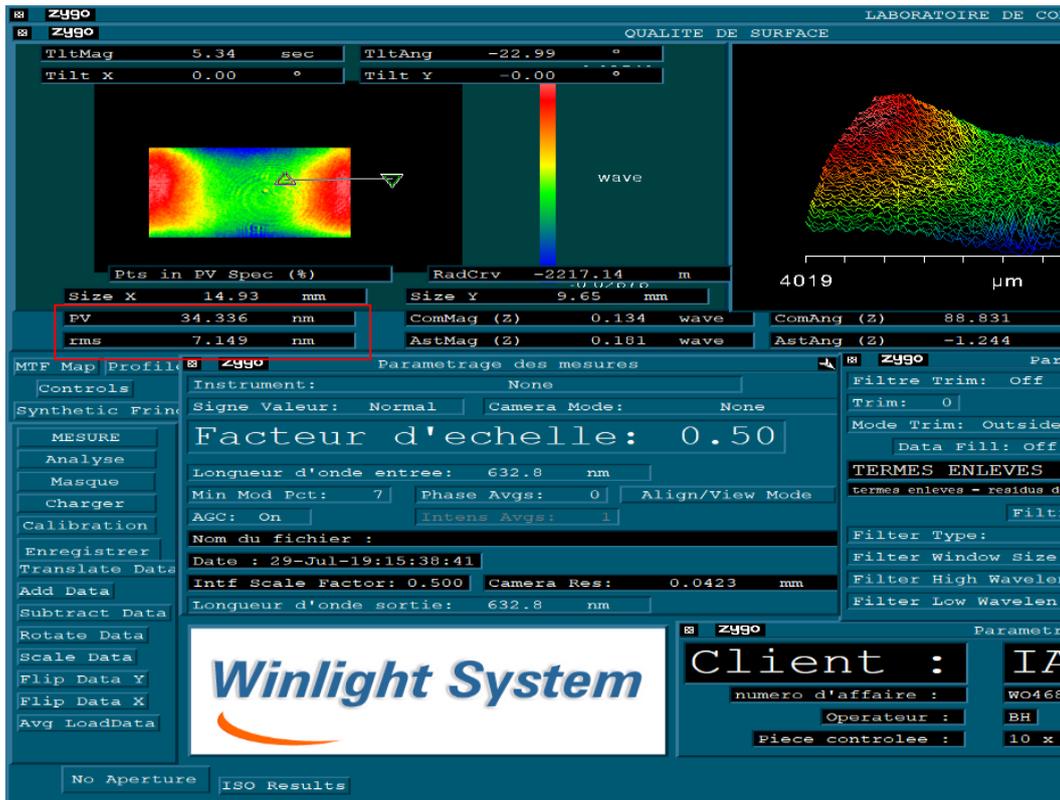
The slices thinning has been done in three major steps:

- Phase 1: Slices shaping
 - 80 slices polished with surfaces compatible for the future optical contacting with respect to the parameters:
 - 2 polished surfaces
 - Cross section: 10 x 15mm
 - Approximately 2mm thick
 - Parallelism compatible with next phase
- Phase 2: Slice thinning
 - 60 polished and thinned to 0.07mm and 0.05mm
 - 2 polished surfaces
 - Cross section: 10 x 15mm
 - Approximately 70µm or 50µm thick depending of the polishing batch
 - Parallelism less than 5µrd
- Phase 3: Front surface shaping
 - Approximately 40 slices

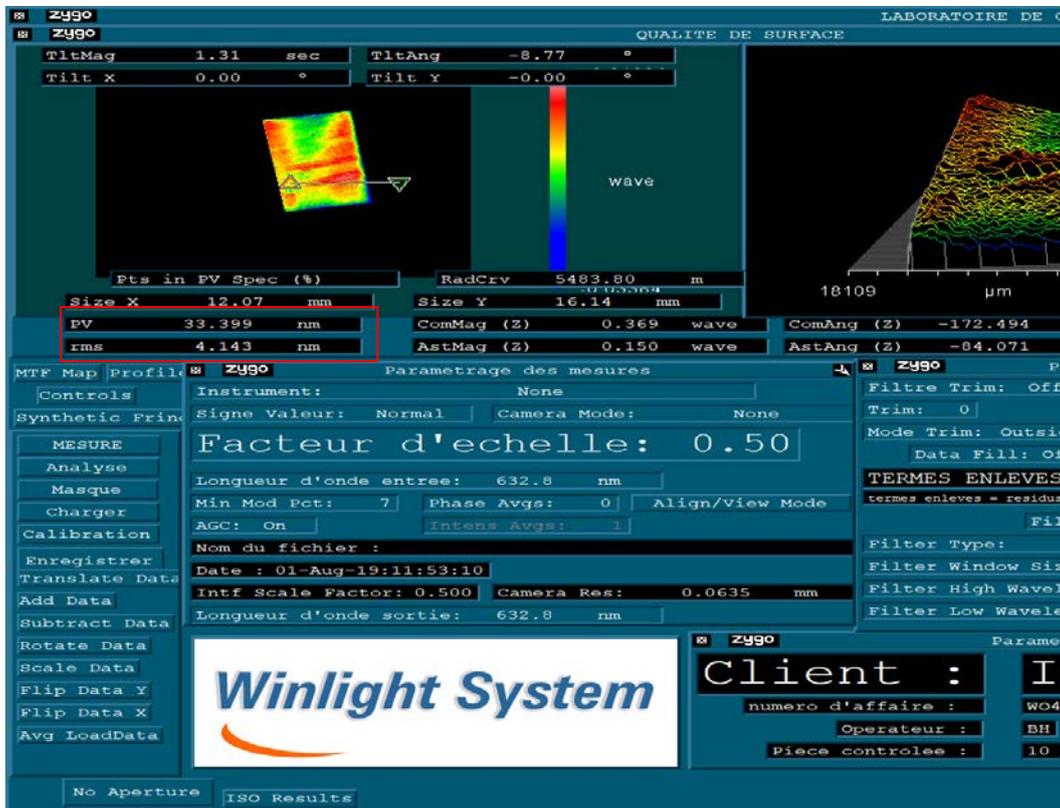
6.1.1 Phase 1: Slices shaping

The table below shows the results of the slices shaping prior to the final 70µm or 50µm thinning step.

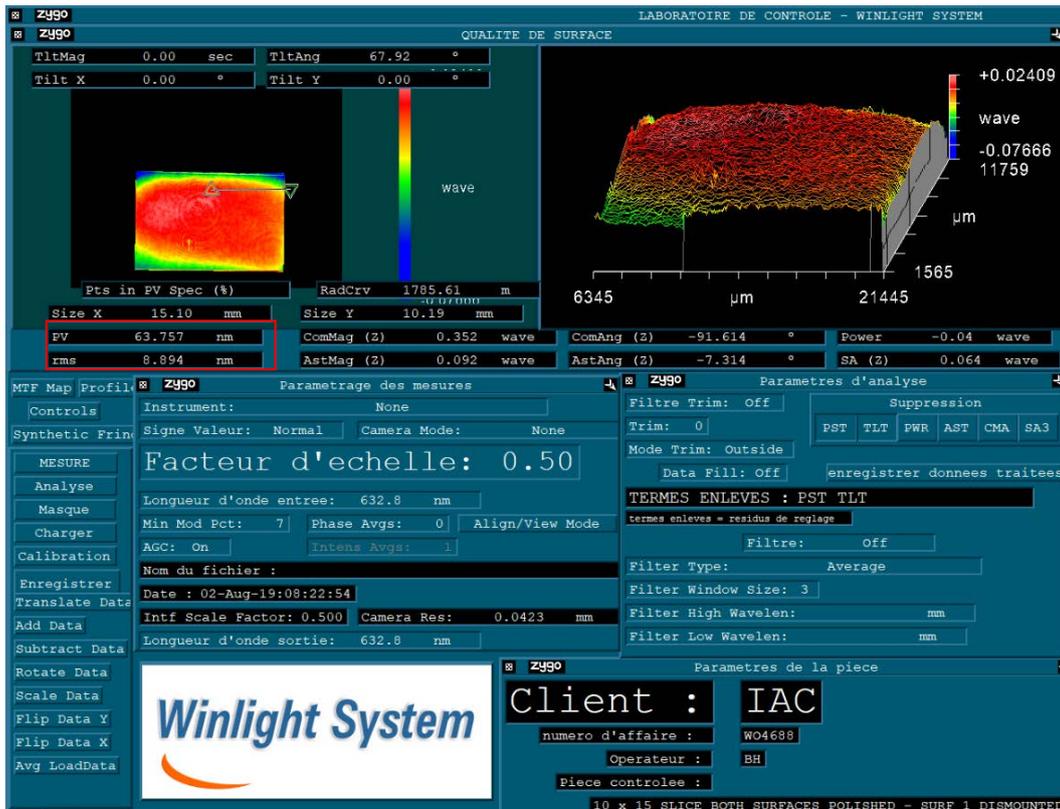
Process results (on 2 runs of 40 slices)	Results on more than 80 slices
After 1 st surface polishing (Component alone)	< 8nm RMS < 50nm PTV
After 2 nd surface polishing (component on the polishing block)	< 8nm RMS < 50nm PTV
After discontacting (surfaces 1 and 2)	< 15nm RMS on both surfaces < 80nm PTV on both surfaces



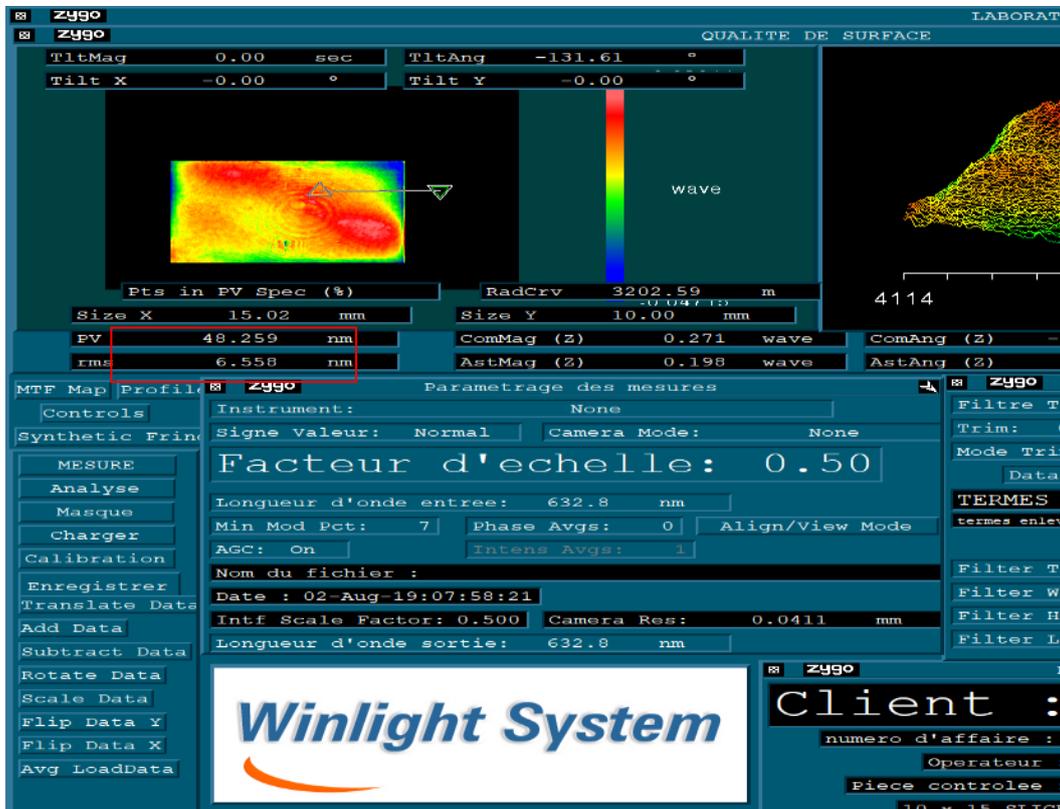
Measurement of a 10 x 15 dismantled slice after first surface polishing



Measurement of a 10 x 15 mounted slice after second surface polishing (optically contacted on polishing block)



Measurement of surface 1 – Slice SN1 10 x 15 dismantled after both surface polishing



Measurement of surface 2 – Slice SN1 10 x 15 dismantled after both surface polishing

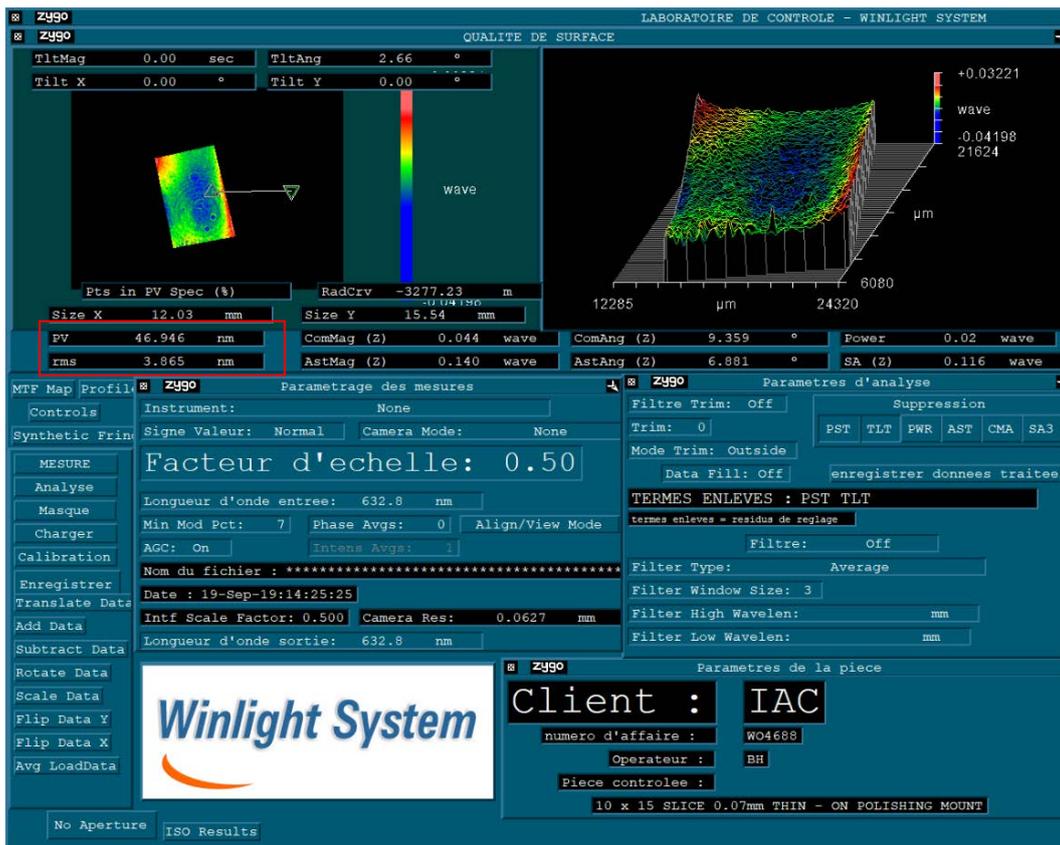
6.1.2 Phase 2: Slices thinning

During this phase, the slices 10 x 15mm 2mm thick have been thinned to 0.07mm and 0.05mm.

Four runs of 15 slices each have been processed to find a coherent and reliable process:

- 3 blocks of 15 slices thinned to 0.07mm
- 1 block of 15 slices thinned to 0.05mm

Process results: thickness 0.07mm (on 3 runs)	Results on 45 slices
After 1 st surface polishing (Component alone)	< 15nm RMS on both surfaces < 80nm PTV on both surfaces
After 2 nd surface polishing (component on the polishing block)	SFE <<10nm RMS SFE <50nm PtV . Thickness: from 0.070 to 0.071mm
After discontacting (surfaces 1 and 2)	The SFE is not measurable because of the slice flexibility.



Measurement of one slice of 10 x 15mm - 0.07mm thick on the polishing bloc n°2

Process results: thickness 0.05mm (on 1 run)	Results on 15 slices
After 1 st surface polishing (Component alone)	< 15nm RMS on both surfaces < 80nm PTV on both surfaces
After 2 nd surface polishing (component on the polishing block)	SFE << 10nm RMS SFE < 50nm PTV Roughness: < 1nm RMS
After discontacting (surfaces 1 and 2)	The SFE is not measurable because of the slice flexibility.



Measurement of one slice of 10 x 15mm - 0.05mm thick on the polishing bloc n°3

Manipulation of the slices:

After development phases and several tests, we have found a solution to handle and stack the 0.05mm and 0.07mm slices without breaking them.

6.1.3 Phase 3: Front surface shaping

6.1.3.1 Thickness 70µm

To process to the front surface shaping, 2 polishing blocs have been assembled, one containing 23 slices and the second 14 slices.

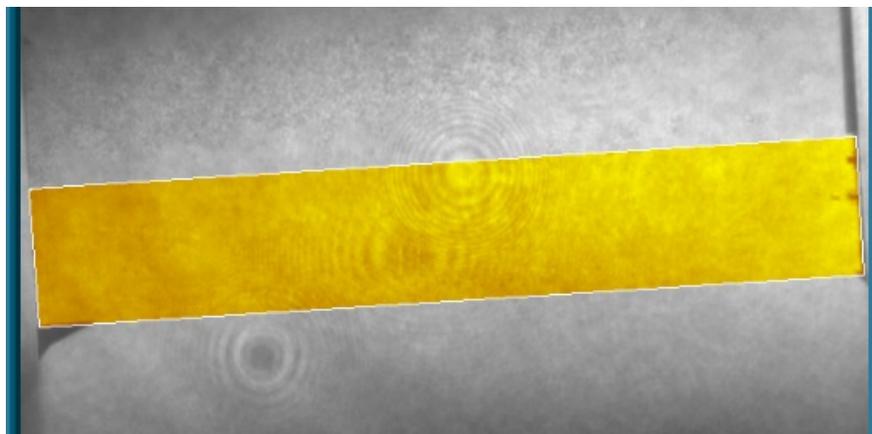
The front surface polishing of the two blocs resulted to high accuracy surfaces with good optical quality.

There are still some remaining defects on the sides of the slices because the sides of the slices were not polished for the test plan. Small chips have been created during the front surface polishing step but there are located on the extreme sides of the 10mm length of the slices. These chips have no impact at all the useful area.

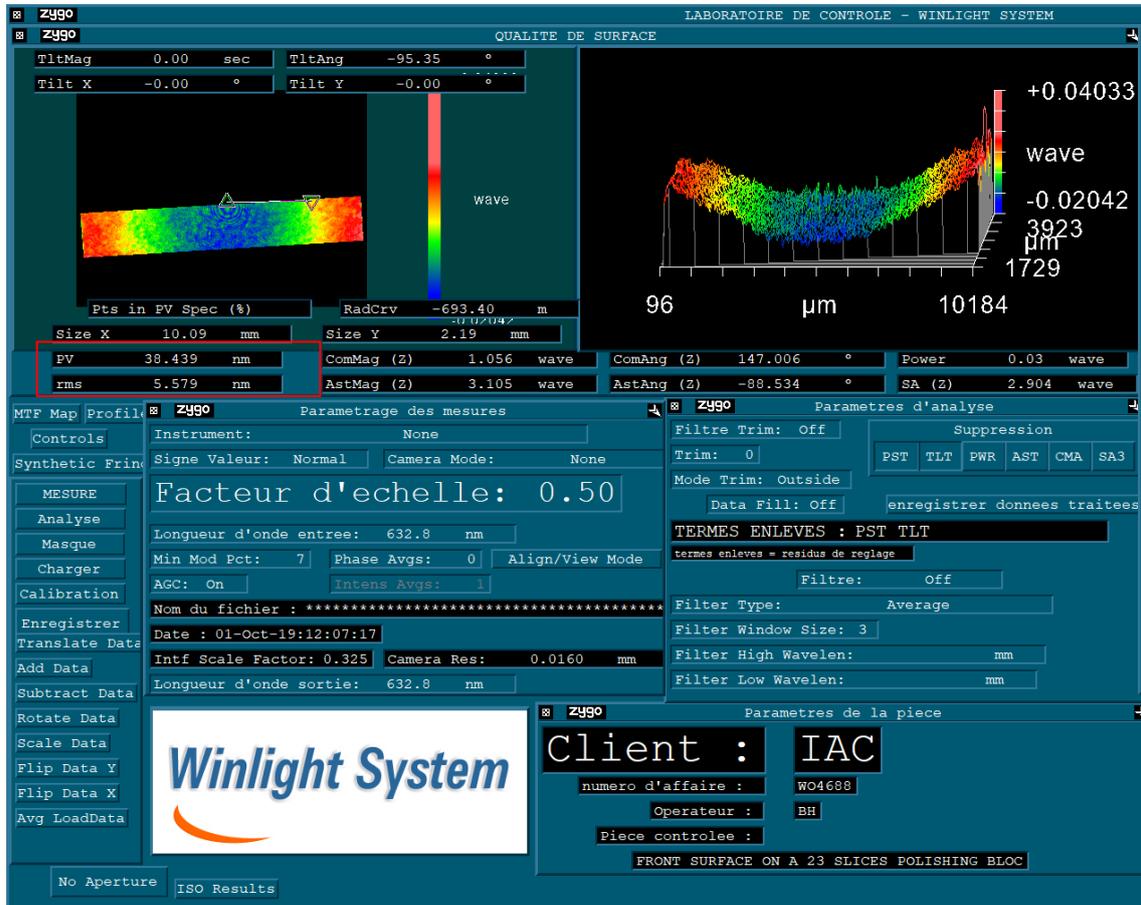
Reminder: for positioning reason, the sides of the slices will be polished for the slicer manufacturing and therefore these defects will not be created on the actual slices.

Slices samples front surface shaping results:	
1 st and 2 nd polishing block	Results on all 0.07mm-thick slices (37 slices)
Surface polishing (component on the polishing block)	<p>SFE on full aperture << 10 nm RMS SFE on full aperture < 50 nm PTV</p> <p>Roughness: < 0.5 nm RMS</p> <p>Cosmetic quality on UA < 10/5</p> <p>Edges: no chips on the top and bottom edges of the slices.</p> <p>As described above, there are some chips on the right and left edges.</p>
After discontacting (if possible)	Non-measurable, the slices are too thin, and too flexibles (*)

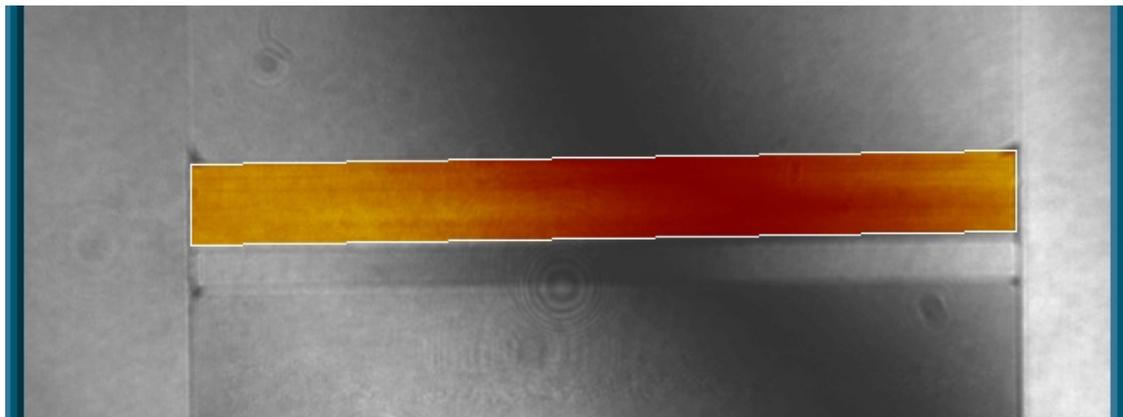
(*) The final SFE measurement will be measured after coating and stacking (slicer stack).



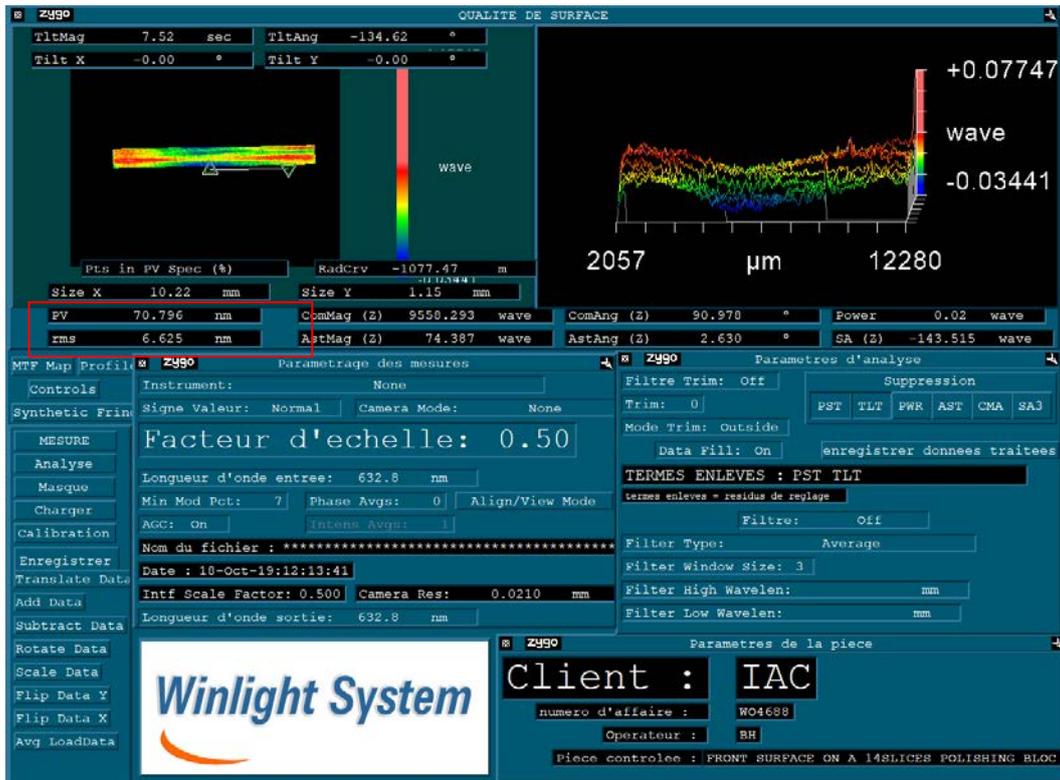
Measurement of a stack of 23 slices (scale ≈ 10)



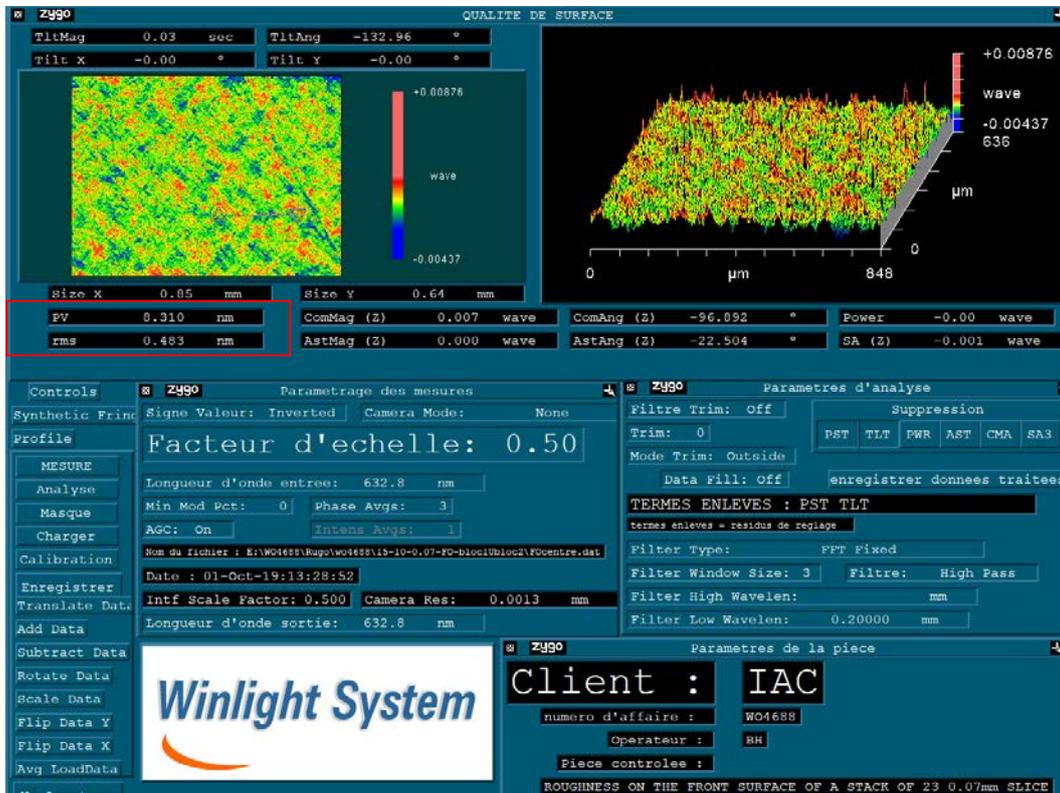
Flatness measurement of the first stack of 23 slices – full aperture



Measurement of a stack of 14 slices Measurement of a stack of 23 slices (scale ≈ 10)



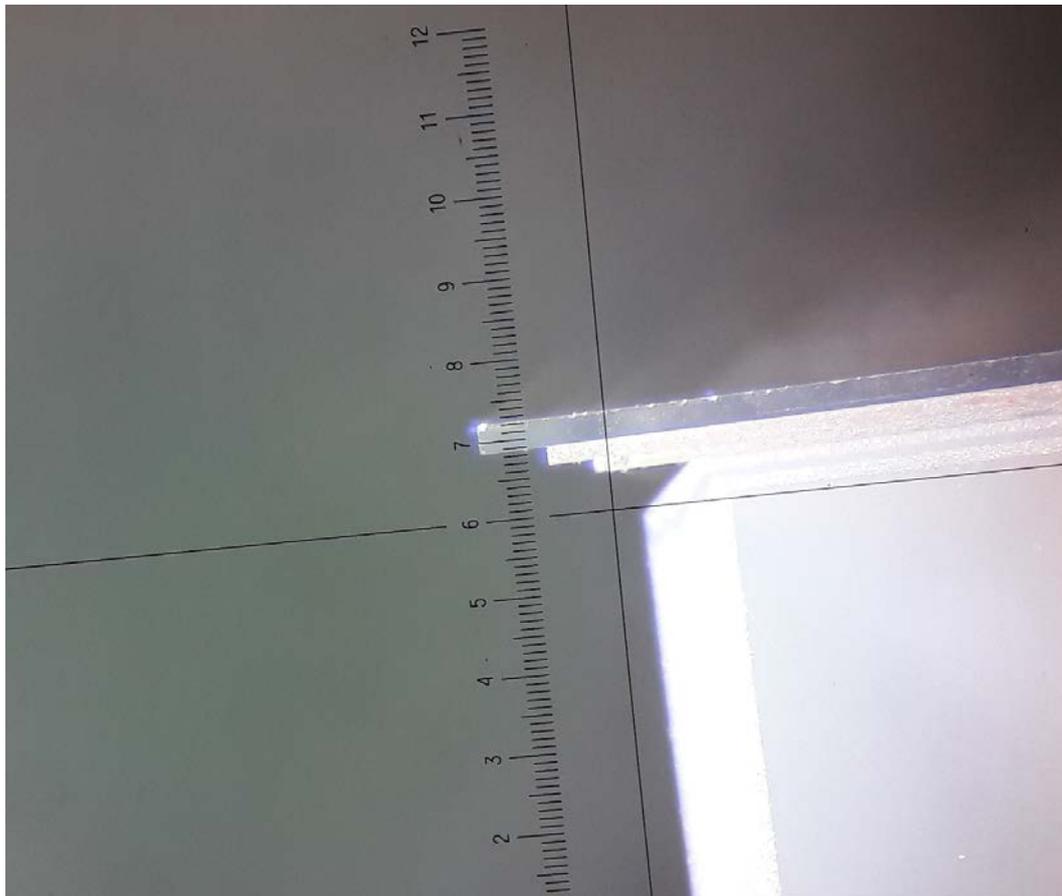
Flatness measurement of a stack of 14 slices – full aperture



Roughness measurement of front surface polishing bloc - stack of 23 slices

6.1.3.2 Thickness 50 μ m

The phase for disconnecting the 50 μ m slices has been validated using specific process to keep the slice integrity. The handling and cleaning process have been reproduced several times to demonstrate the reliability of the manufacturing process for such slices.



*Example of stacking (from above to below)
(Slice 100 μ m thick, slice 70 μ m thick, slice 50 μ m thick)*

6.2 Final stacking

6.2.1 Stacking 70 μ m thick slices

We built 2 coated stacks of slices to validate the final stacking. One was constituted with 3 slices and the second one constituted with 10 slices.

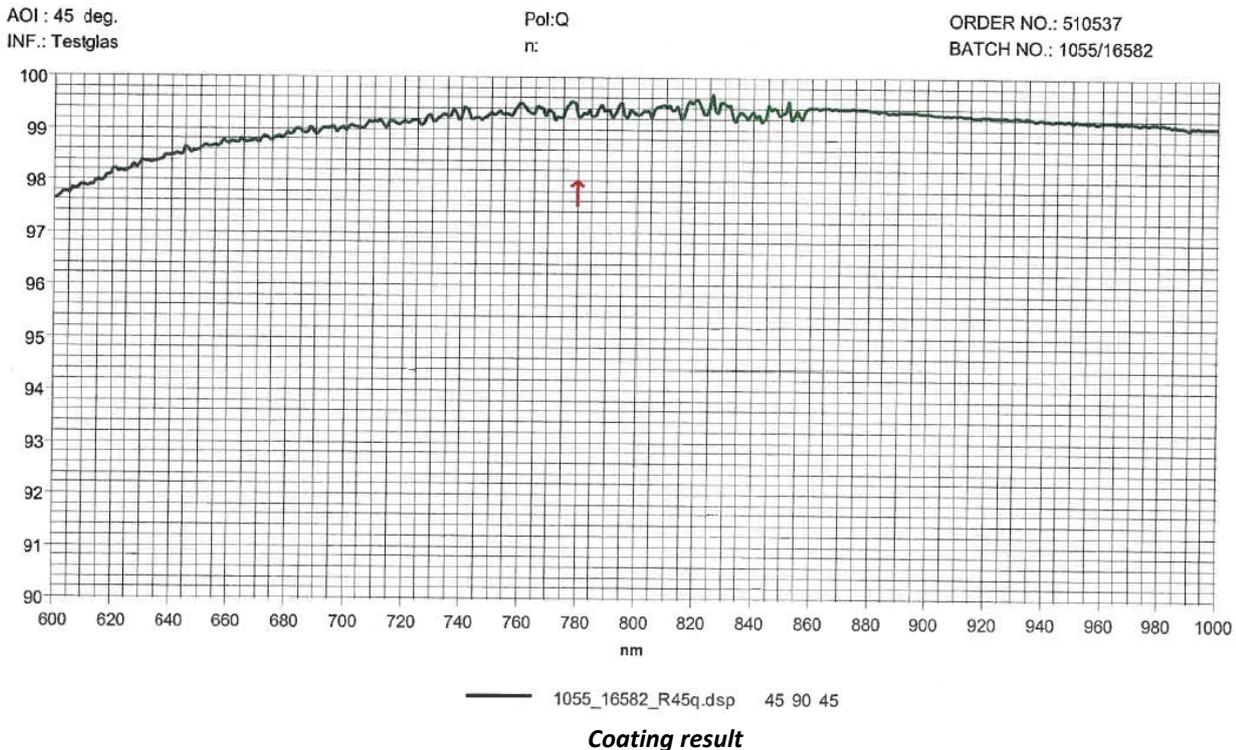
- Stack 1 used for manipulation and positioning tests
- Stack 2 used to demonstrate the feasibility of stacking 10 slices.

The two stacks have been thermally cycled prior to do the final measurements

- 10 loops +70°C / -55°C
- 3 loops 20°C / -195°C

Slicer stacks front surface shaping results: (After coating and thermal cycling)	
1 st and 2 nd polishing block	Results on 10 slices (70 µm thick) stacked together And 3 slices (70 µm thick) stacked together
Environment resist	10 loops +70°C / -55°C 3 loops 20°C / -195°C Climatic tests for coating
Roughness	Roughness: < 0.7 to 1nm RMS
Surface front error On aperture (70x1000µm ²)	From 18nm PTV to 25nm PTV From 2.2nm RMS to 3.8nm RMS
Surface front error On aperture (70x500µm ²)	From 19nm PTV to 31nm PTV From 1.9nm RMS to 5.4nm RMS
Coating	The coating covers all the active surfaces. There is no lack of coating and there is no edge effect The flatness and the roughness are not degraded by the coating
Cosmetic quality	No scratch and dig > 10/5 Sharp edges: size maxi of the chips = 5µm (*) As described above, there are some chips on the right and left edges.

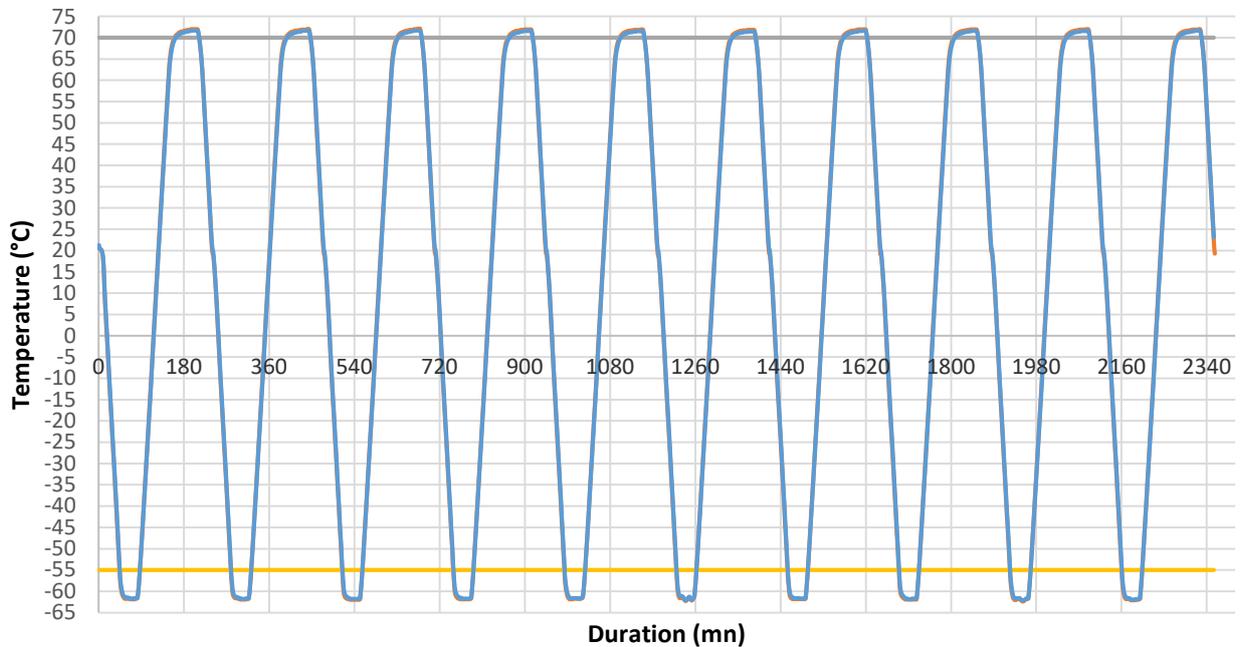
(*) The defaults seen on the next pages pictures are diffusing elements revealed by an incident light. In normal condition, most of these defaults are not visible.



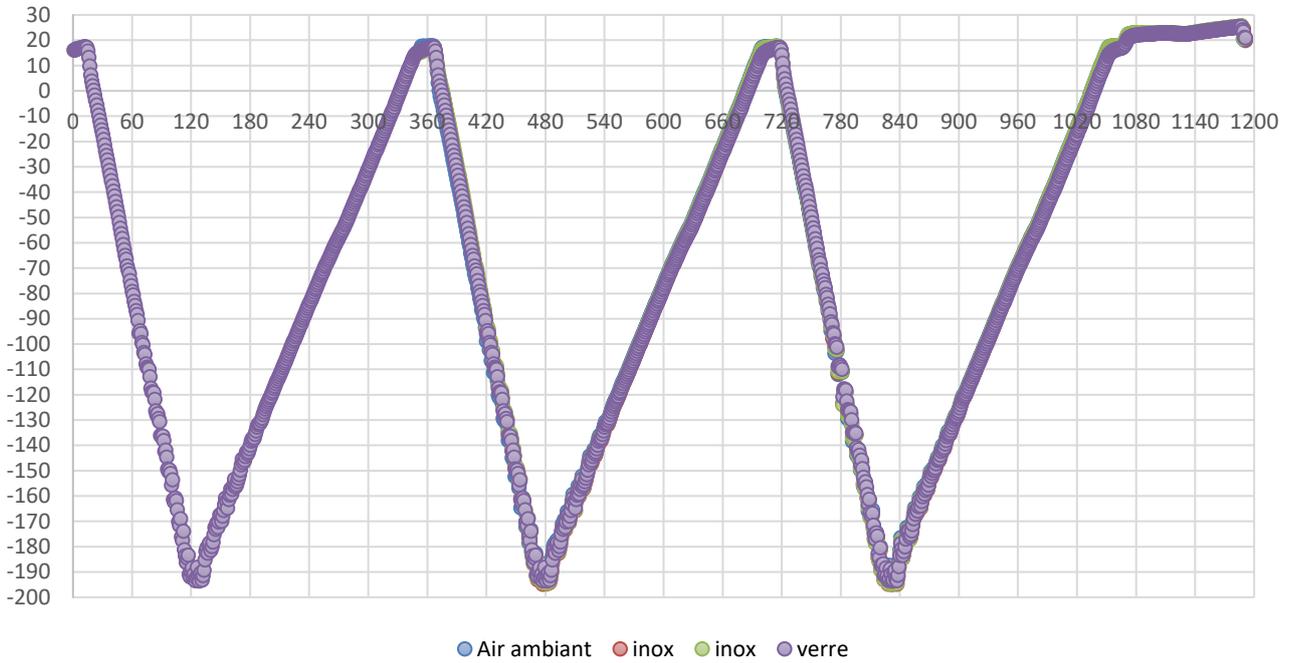
Successful tests applied on slicer stacks and witness samples

- Adhesion: Pulling test 15sec / 25mm normal to the surface (on witness samples)
- Abrasion: 50 movements with cheesecloth 5N+/-1N (on witness samples)
- Humidity: 24H à 45°C - 95 à 100% relative humidity (on slicers stacks and witness samples)
- Solubility: Immersion in deionized water 23°C/6H (on slicers stacks and witness samples)
- Thermal cycles: **(on slicers stacks and witness samples)**
 - Temperature +60°C within 0.5H
 - Temperature -10°C within 0.5H
 - slopes +60°C to -10°C: 60°C/H
 - 27 cycles

Thermique cycling applied on slicer stacks 10 loops +70°C / -55°C



Cryo tests applied on slicers stacks



LABORATOIRE DE CONTROLE - WINLIGHT SYSTEM

QUALITE DE SURFACE

TitMag	0.03 sec	TitAng	-143.19 °
Tilt X	-0.02 sec	Tilt Y	-0.02 sec

Size X: 63.56 μm Size Y: 1014.89 μm

PV: 7.584 nm rms: 0.753 nm

ComMag (2): 30.357 wave AstMag (2): 45.726 wave

ComAng (2): 145.996 ° AstAng (2): -89.315 °

Power: -0.00 wave SA (2): 36.693 wave

Facteur d'echelle: 0.50

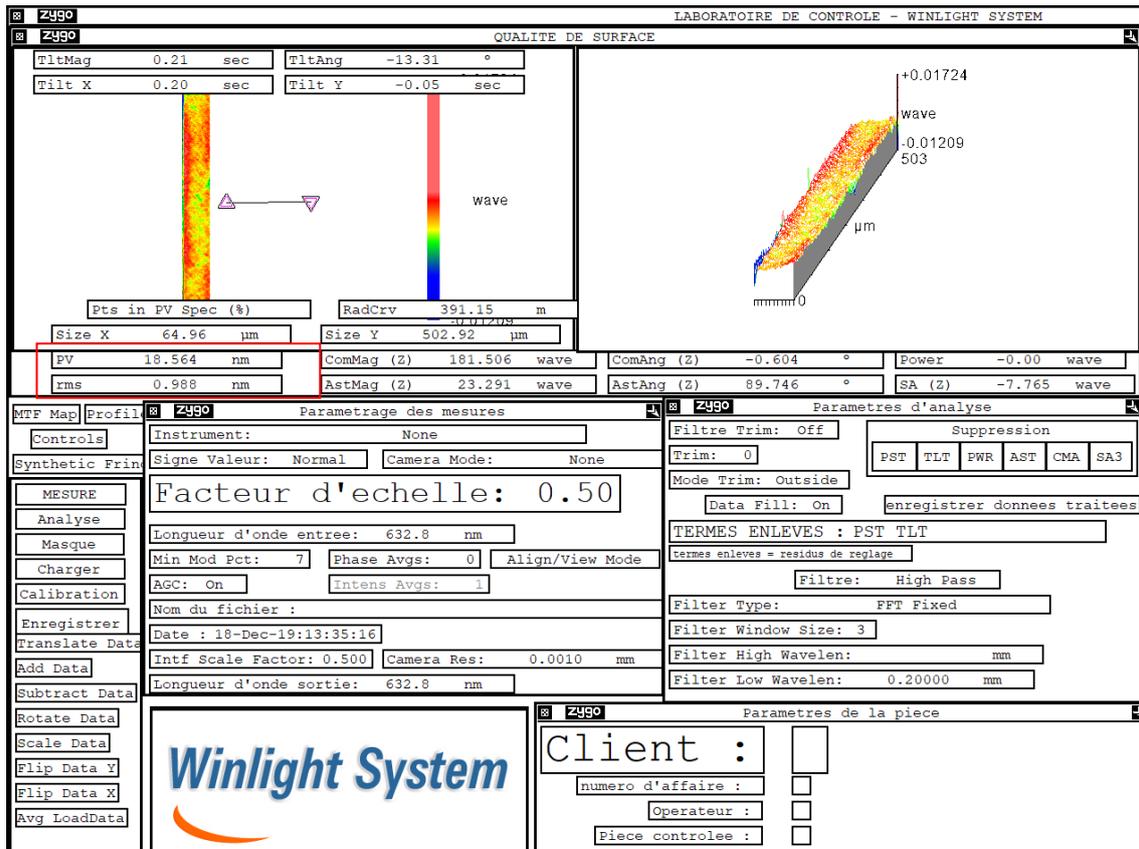
Longueur d'onde entree: 632.8 nm Longueur d'onde sortie: 632.8 nm

Min Mod Pct: 7 Phase Avgs: 0 Intens Avgs: 1

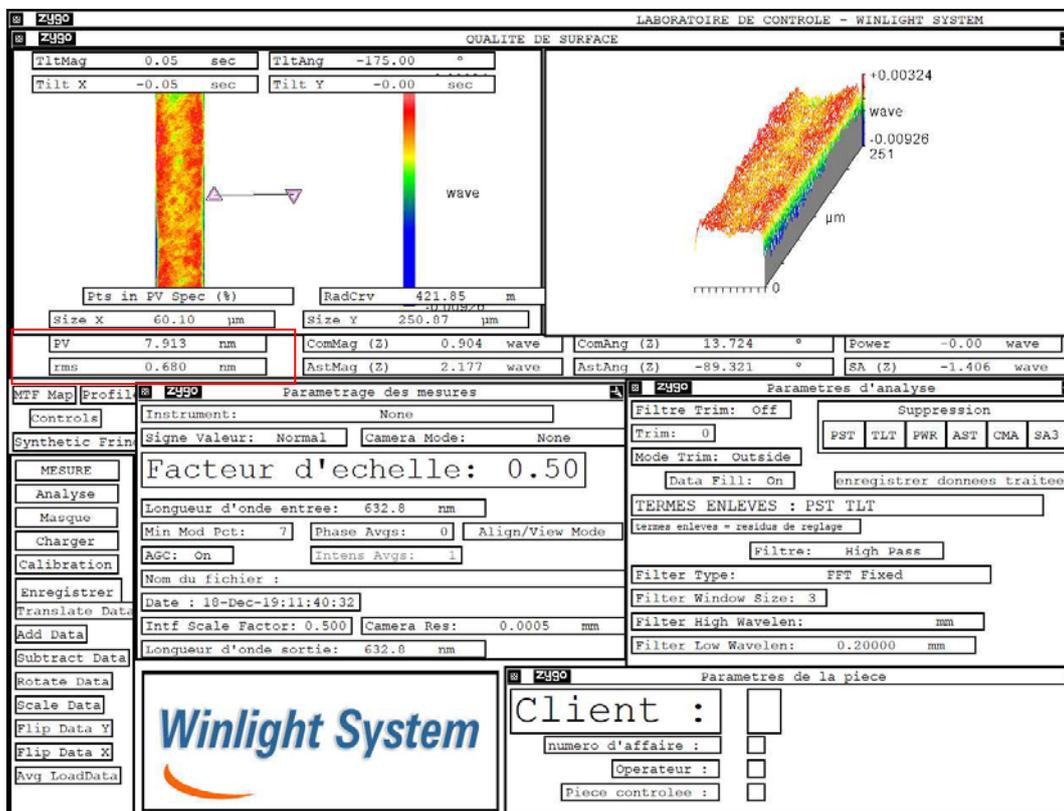
Camera Res: 0.0021 mm

Client :
 numero d'affaire :
 Operateur :
 Piece controlee :

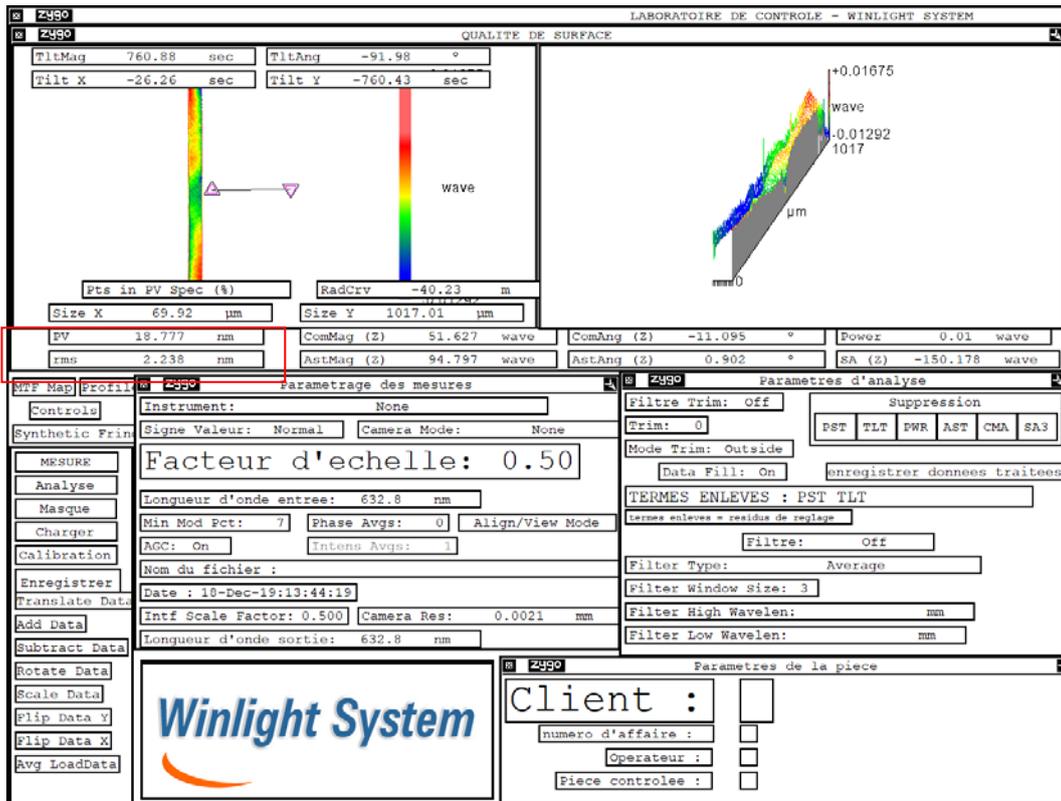
Example of roughness measurement on 1 slice stack 1 (area 60x1000 μm)



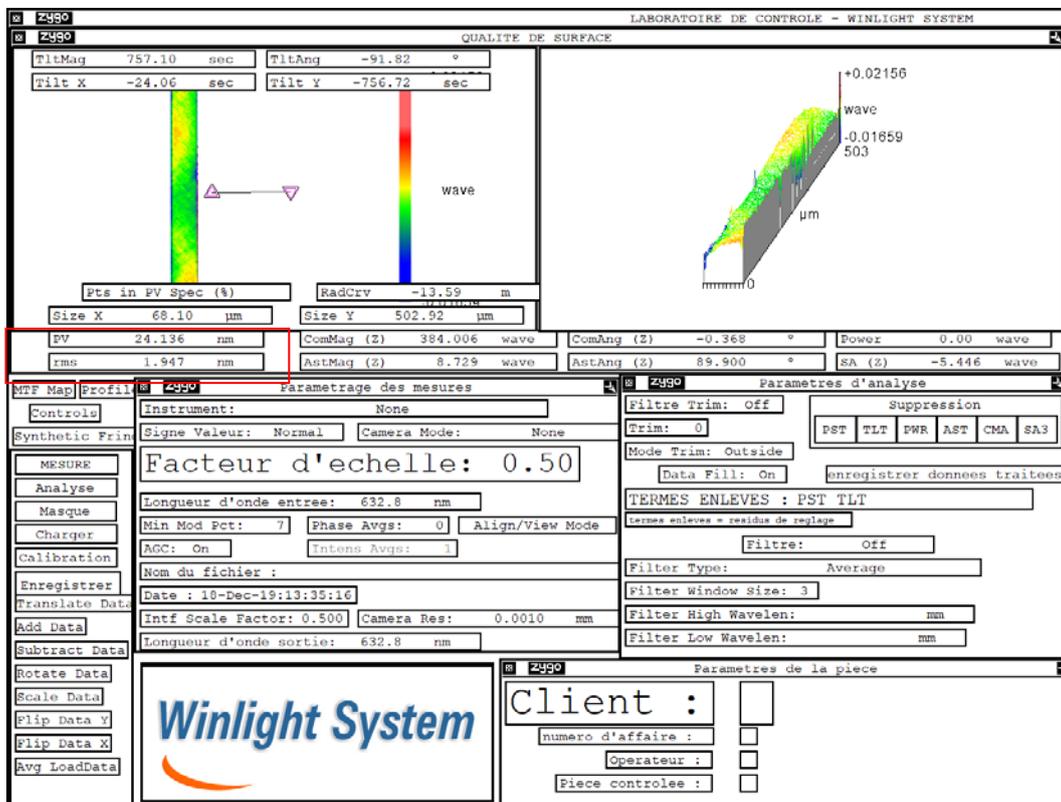
Example of roughness measurement on 1 slice stack 2 (area 60x500µm)



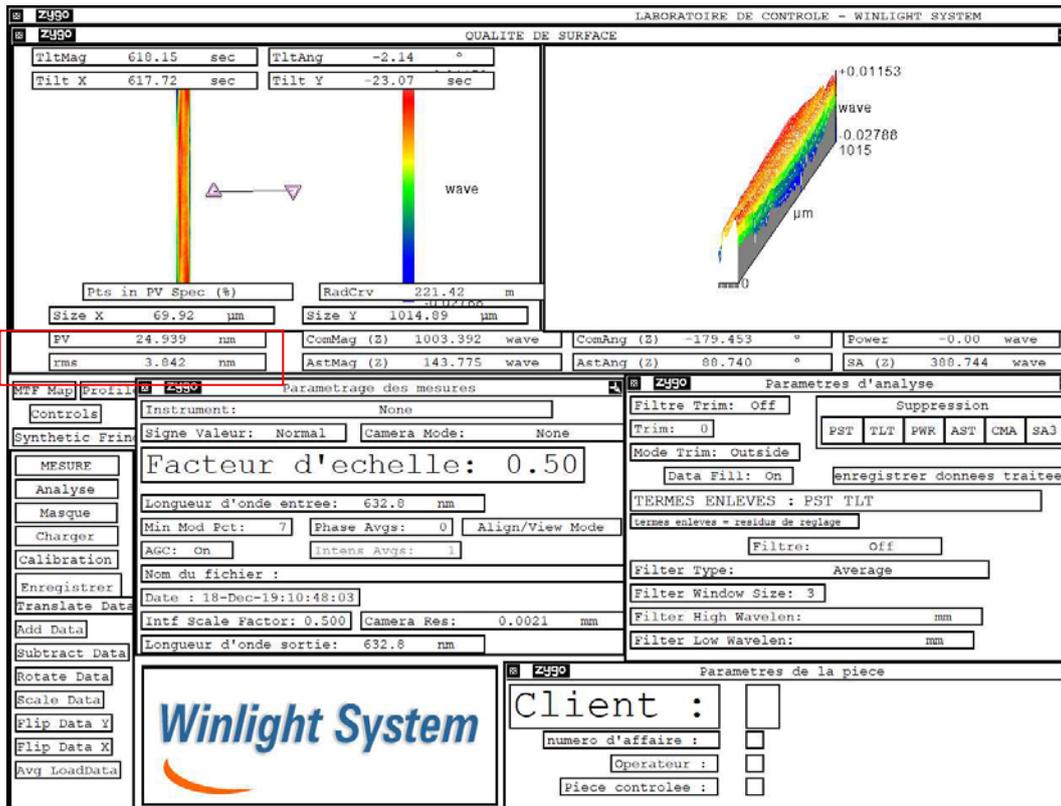
Example of roughness measurement on 1 slice stack 1 (area 60x250µm)



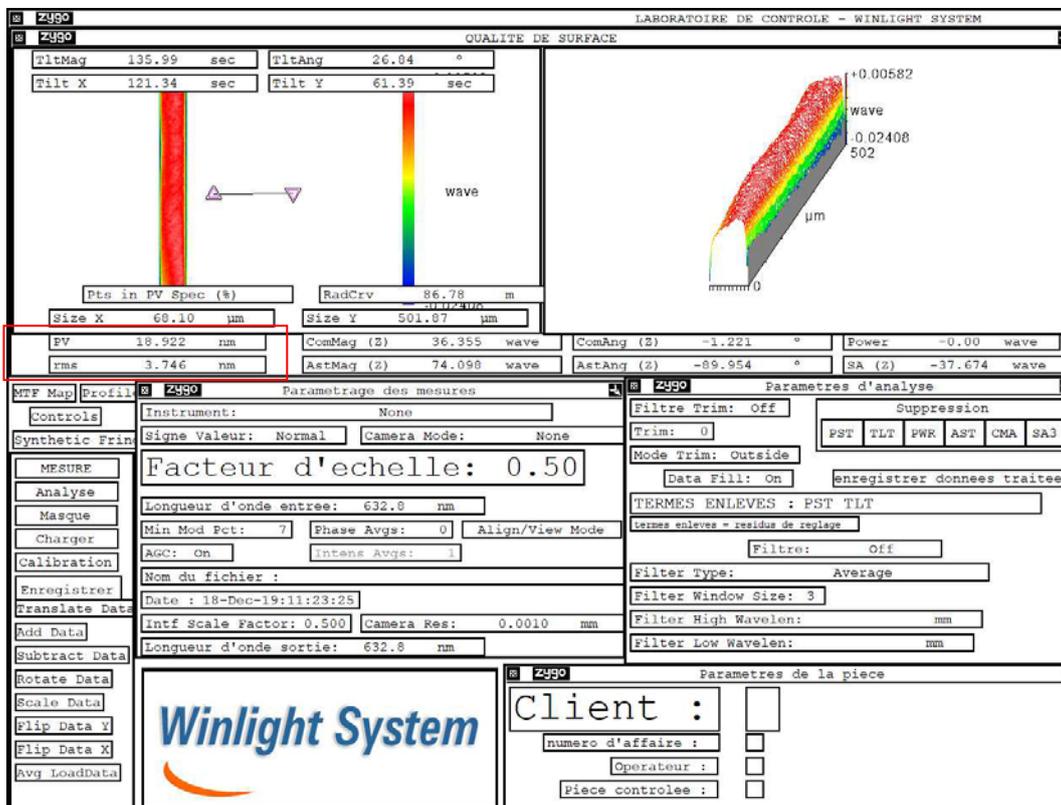
Example of SFE measurement on slice2 stack1



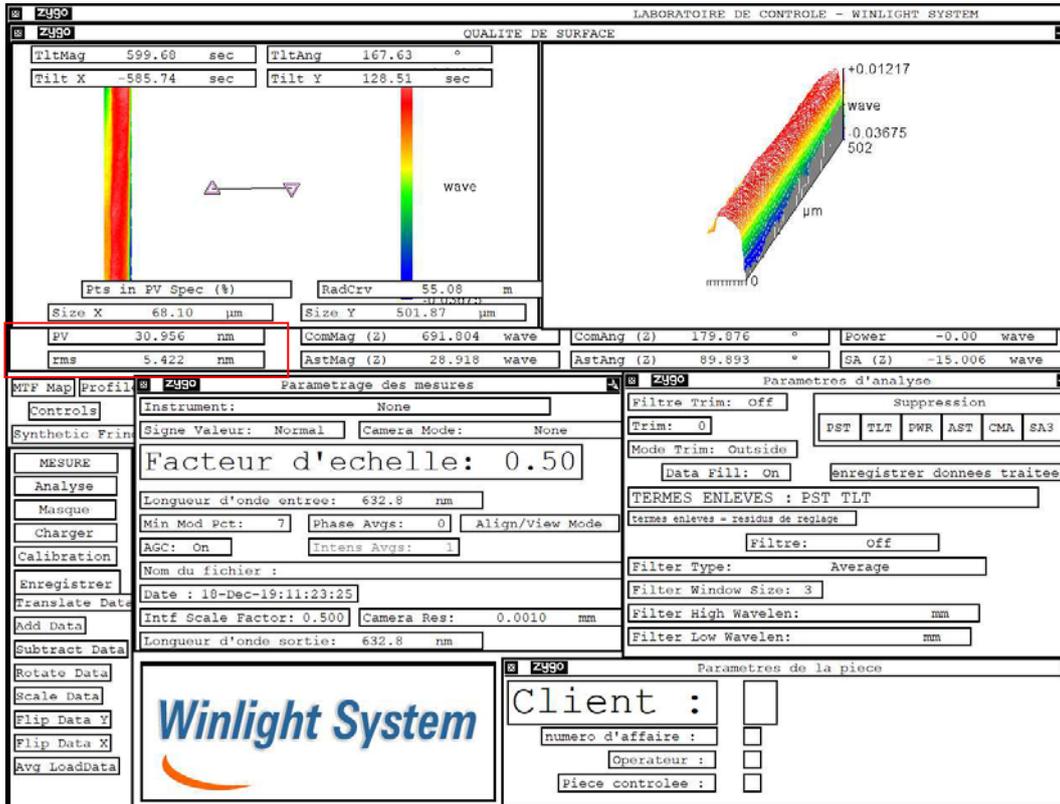
Example of SFE measurement on slice8 stack2



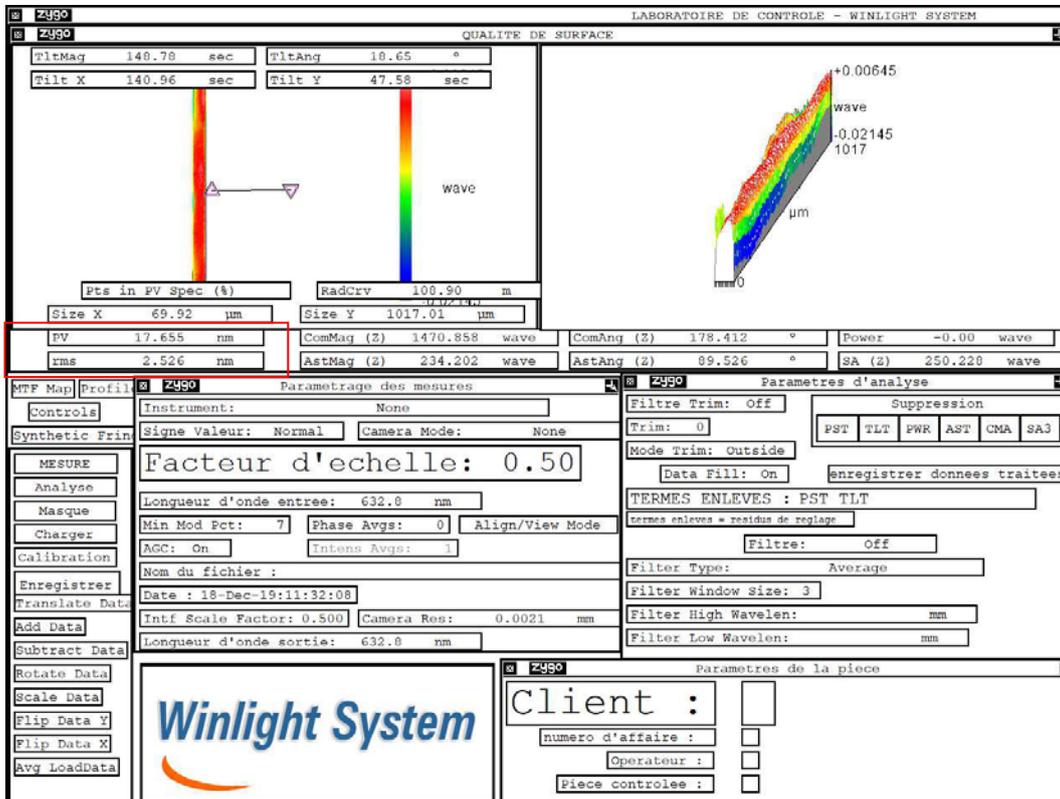
Example of SFE measurement on slice3 stack2



Example of SFE measurement on slice2 stack1

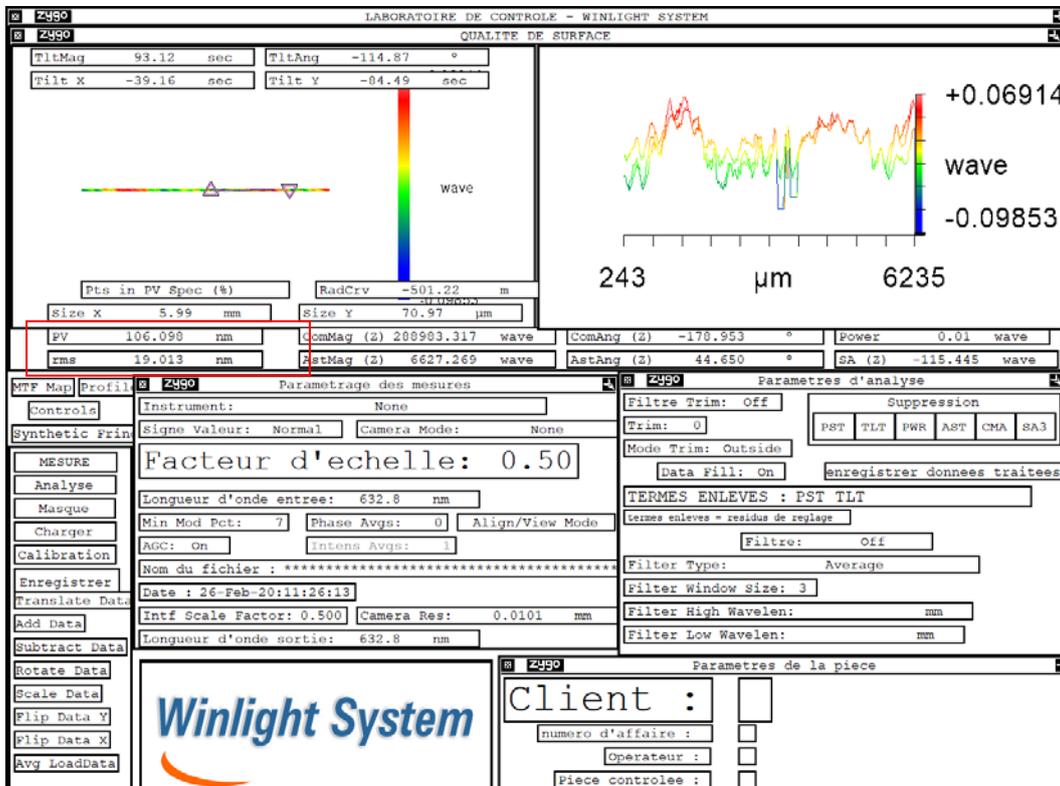


Example of SFE measurement on slice1 stack1

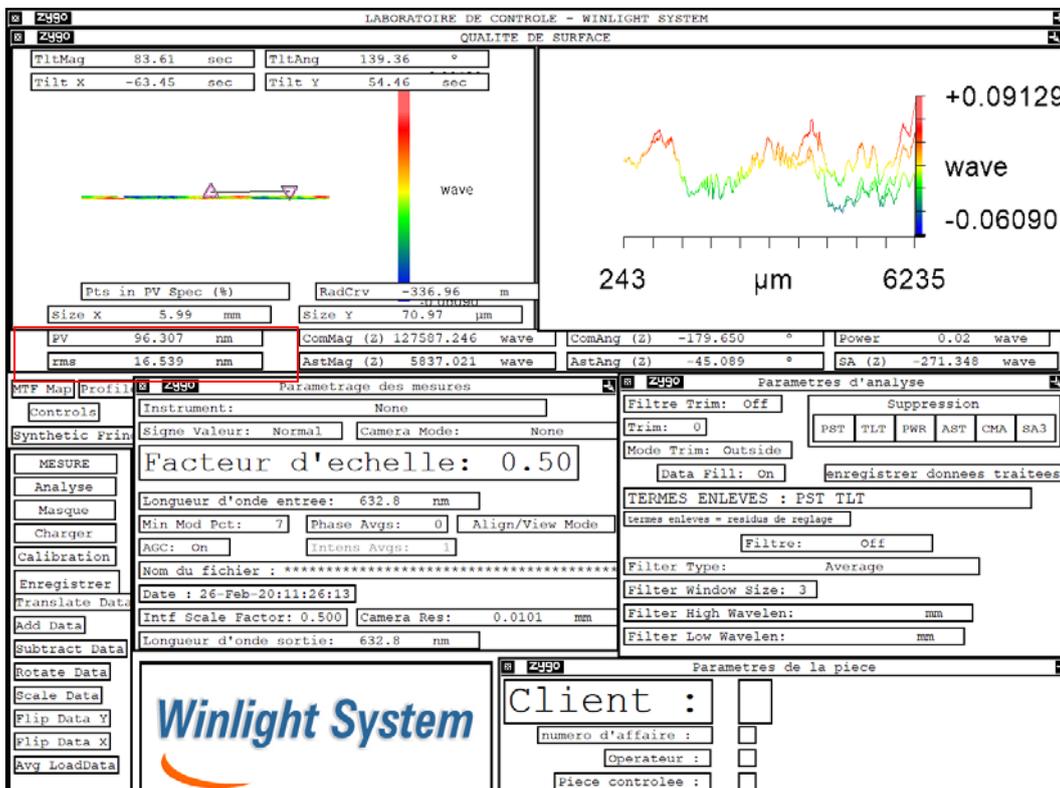


Example of SFE measurement on slice2 stack1

Examples of SFE on 6mm x 70µm

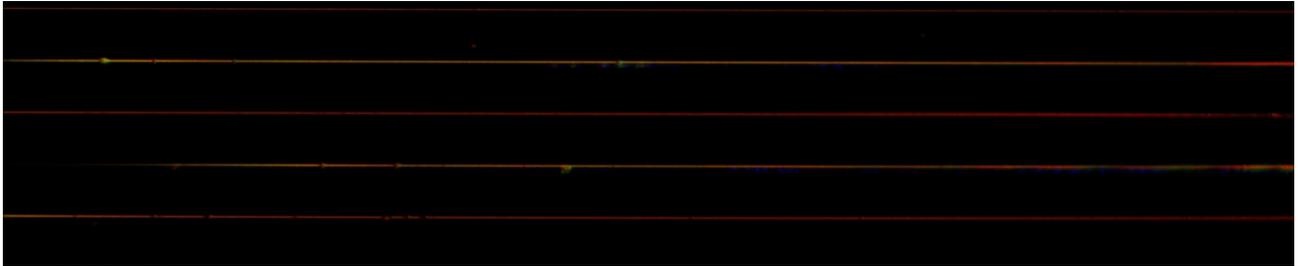


Example of SFE measurement on slice1 stack2

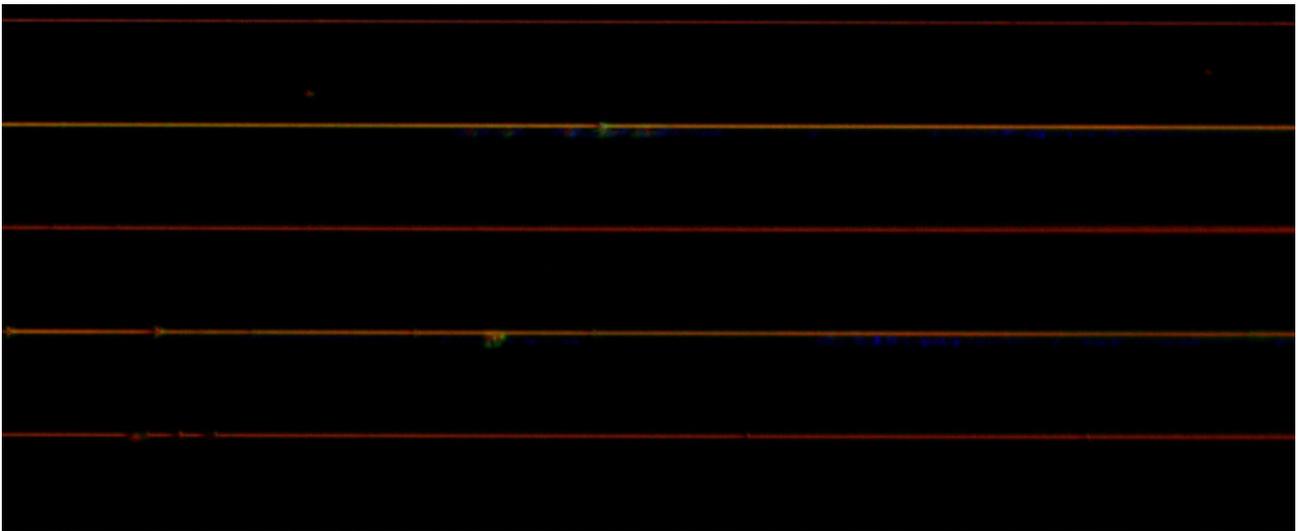


Example of SFE measurement on slice1 stack2

STACK 1

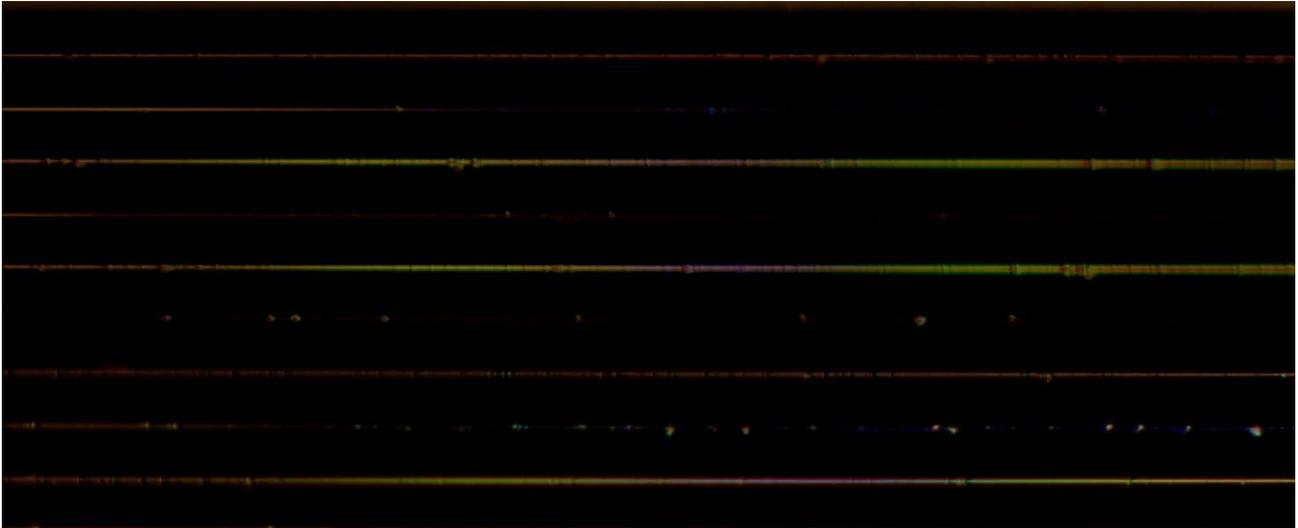


*Front surfaces of the slices after coating Stack 1 (5 slices 0.07*1.6mm)*

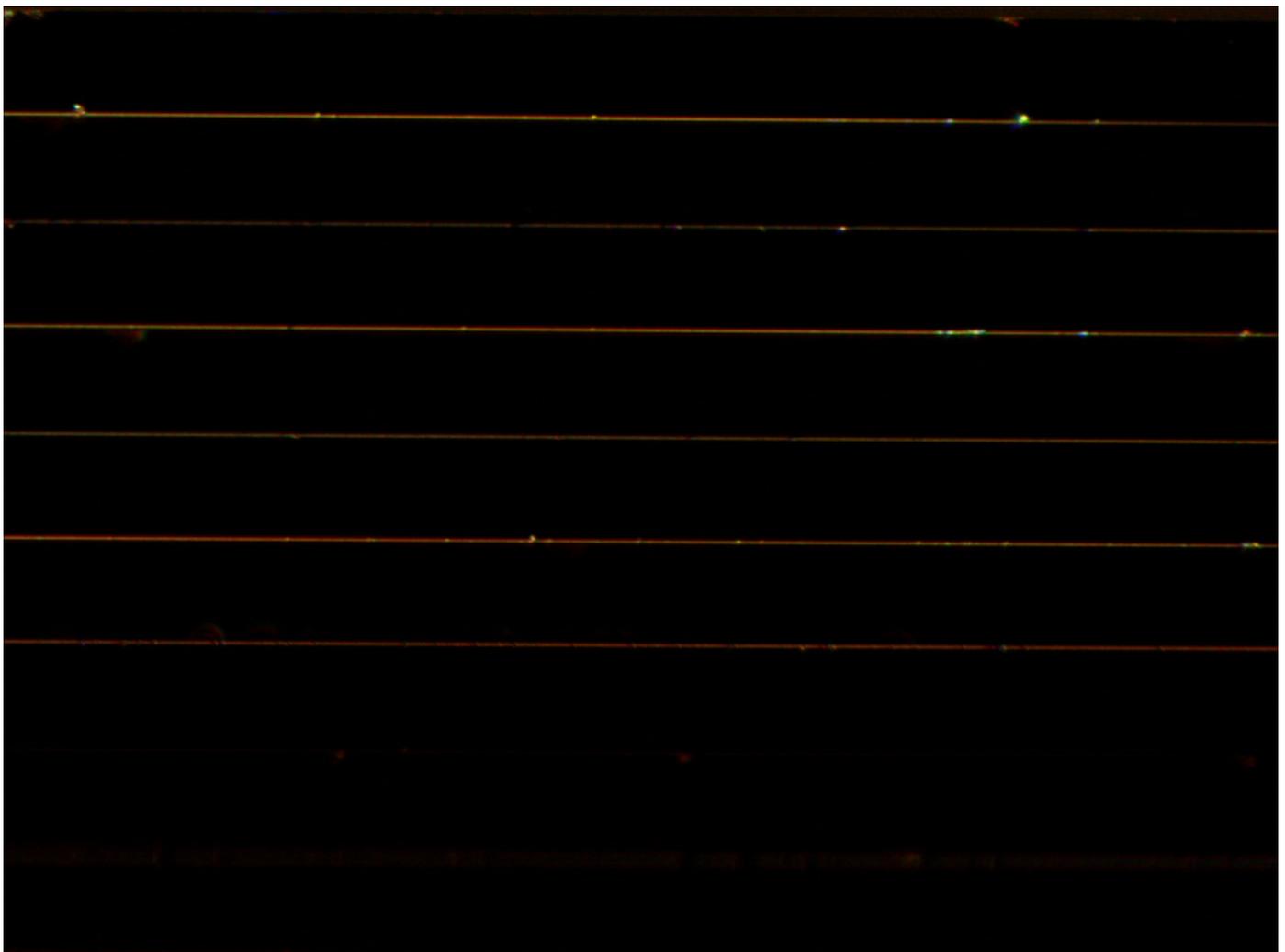


*ZOOM Front surfaces of the slices after coating stack 1 (5 slices 0.07*0.8mm)*

STACK 2



*Front surfaces of the slices after coating Stack 2 (10 slices 0.07*1.6mm)*



*ZOOM Front surfaces of the slices after coating stack 2 (10 slices 0.07*0.8mm)*



Profile of the stack with 10 slices (We see what we explained before, the effect of the unpolished sides)



Profile of the stack with 5 slices (We see what we explained before, the effect of the unpolished sides)

7 Conclusion

This report demonstrates that WINLIGHT SYSTEM is capable to manufacture and integrate such thin slices within the tolerances:

Item	Result
Thinning	Thickness 70µm: SFE < 25nm RMS, compatible with optical contacting Thickness 50µm: SFE < 25nm RMS, compatible with optical contacting
Front surface shaping	SFE < 20nm RMS, Rq < 1nm RMS No chip > 10µm, 5µm > 1 chip > 10µm, 1µm > 5 chips > 5µm
Final stacking	Slices 70µm thick: SFE < 20nm RMS for 6mm long <ul style="list-style-type: none"> ➤ Chip 10µm: qty 1 at maximum ➤ 5µm < Chips < 9µm: qty max 2 ➤ 2µm < Chips < 4µm: qty max 10 ➤ Chips < 2µm: Qty not measured Slices 50µm thick: No concern for the manipulation and stacking
Coating	Coating compatible with such thin tilted slices Coating compatible with thermal environments
Stability	Stability after 10x +70°C/-55°C and 3x -195°C/20°C

This report demonstrates the ability of WINLIGHT-SYSTEM to meet a reliable slice thinning process.

8 Open points

None